REMARKS

The Office Action mailed March 12, 2004, has been received and reviewed. Claims 1 through 7, 9 through 16, and 18 through 20 are currently pending in the application. Claims 1 through 7, 9 through 16, and 18 through 20 stand rejected. Applicant has amended claims 1 and 13, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in view of U.S. Patent No. 5,909,559 to So and further in view of U.S. Patent No. 6,246,719 to Agarwal

Claims 1 through 5, 7, 10, 12 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Agarwal (U.S. Patent No. 6,246,719). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Applicant asserts that the 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 5, 7, 10, 12 and 20 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Independent Claim 1

Applicant's invention as claimed includes separate interfaces to a shared memory. Data is directly placed in the memory by a result buffer over a first bus and then data is retrieved from the memory by a central processing unit through a north bridge chip without burdening the system or second bus. Applicant's independent claim 1, reads in part:

> 1. An apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising:
> a video input port . . .;
> a video input buffer . . .;
> a previous frame buffer . . .;
> an operation unit . . .; and
> a result buffer coupled to the operation unit, the ***result buffer further including a memory interface configured to couple with the system memory via a first bus*** independent of ***a second bus configured for coupling with the central processing unit via a north bridge chip***, the result buffer for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the apparatus configured to operate within the north bridge chip of the computer system to enable the central processing unit ***to retrieve*** the difference frame ***exclusive of the second bus and directly from the system memory via the north bridge chip*** for further compression of the video data by the central processing unit.

The Office Action concedes that:

> Dea does not explicitly disclose: 1) the claimed the result buffer further including memory interface configured for coupling with the system memory via a first bus independent of a second bus configured for coupling with the central processing unit, and 2) the claimed apparatus configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit. (Office Action pp. 4-5).

Therefore, any such teaching must be found in the newly cited reference, Agarwal. That is to say, Agarwal would have to teach or suggest the missing elements of Applicant's presently amended independent claim 1, namely

> a result buffer coupled to the operation unit, the ***result buffer further including a memory interface configured to couple with the system memory via a first bus***

> independent of ***a second bus configured for coupling with the central processing unit via a north bridge chip***, the result buffer for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the apparatus configured to operate within the north bridge chip of the computer system to enable the central processing unit ***to retrieve*** the difference frame ***exclusive of the second bus and directly from the system memory via the north bridge chip*** for further compression of the video data by the central processing unit.

While the Office Action makes statements that Agarwal teaches the missing elements, the Office Action mischaracterizes the teachings of the Agarwal reference which, in fact, does not teach the missing elements.

While the Office Action states:

> 1) Agarwal teaches that the encoded image may then be stored to memory device 112 via bus 108, bus interface 110, and system bus 114 for storage in host memory 126, pixel processor 106 also may contain local memory 130, which is tightly-coupled on-chip memory suitable for locally storing a number of pixels and other data, those skilled in the art will appreciate that system bus 114 and bus 108 may be merged into the same system bus 114 (Fig. 1, col. 4, lines 20-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention ***to incorporate the two system bus 114 and 108 as taught by Agarwal*** into Dea's system since it merely amount of selecting available buses. (Office Action p. 5; emphasis added).

In referencing Agarwal's Fig. 1, and according to the Office Action's characterization, the data flow is from pixel processor 106, to bus 108, to memory device 112, back to bus 108, to bus interface 110, to system bus 114, to host memory 126. Then, and only then, can host processor 116 retrieve data from host memory 126 for any further performance of video compression. It should be noted that such a retrieval of data necessitates traversal of the system bus at least on two separate occasions. The Applicant's invention as claimed, allows the "central processing unit to retrieve the difference frame exclusive of the second bus and directly from the system memory" wherein the second bus is configured in a manner similar to a "system bus".

While the Office Action and the Agarwal reference state that the "system bus 114 and bus 108 may be merged into the same system bus 114", such a configuration places pixel processor 106, memory device 112, system memory 126 and host processor 116 all on a single system bus

114 which is in contradiction to the lack of teaching of Applicant's claimed invention of:

> a result buffer coupled to the operation unit, the ***result buffer further including a memory interface configured to couple with the system memory via a first bus*** independent of ***a second bus configured for coupling with the central processing unit via a north bridge chip***, the result buffer for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the apparatus configured to operate within the north bridge chip of the computer system to enable the central processing unit ***to retrieve*** the difference frame ***exclusive of the second bus and directly from the system memory via the north bridge chip*** for further compression of the video data by the central processing unit.

Therefore, Applicant respectfully requests that the rejection to amended independent claim 1 be withdrawn. Furthermore, claim 2 through 7 and 9 through 12 depending from amended independent claim 1 are also allowable as depending from allowable amended independent claim 1.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 5,909,559 to So, U.S. Patent No. 6,246,719 to Agarwal and further in view of U.S. Patent No. 4,546,383 to Abramatic et al.

Claims 6, and 13 through 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559), Agarwal (U.S. Patent No. 6,246,719) and further in view of Abramatic et al. (U.S. Patent No. 4,546,383). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant submits that claim 6 is allowable for at least its dependency on allowable amended independent claim 1. Therefore, Applicant respectfully requests the withdrawal of the rejection of claim 6.

Regarding independent claim 13 and claims 14 through 16, 18 and 19 depending therefrom,

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of independent claim 13 and claim 14 through 16, 18 and 19 depending therefrom, are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Independent Claim 13

Applicant's invention as claimed includes separate interfaces to a shared memory. Data is directly placed in the memory by a result buffer over a first bus and then data is retrieved from the memory by a central processing unit through a north bridge chip without burdening the system or second bus. Applicant's independent claim 13, reads in part:

> 13. An apparatus for compressing video data in a computer system including a central processing unit, comprising:
> a video input port . . .;
> a video input buffer . . .;
> a previous frame buffer . . .;
> an exclusive-OR unit . . .;
> a result buffer . . .;
> a memory port coupled to the previous frame buffer and the result buffer, the memory port independent from the video input port; and

a system memory ***coupled to the memory port for storing the video data from the video input port and the difference frame from the result buffer***, wherein the video data is stored to in a current frame in the memory, the apparatus configured to operate within a north bridge chip of the computer system ***to enable the central processing unit via the north bridge chip to retrieve the difference frame exclusive of a system bus directly from the system memory via the north bridge chip*** for further compression of the video data by the central processing unit.

The Office Action concedes that:

Dea does not explicitly disclose the following limitations, . . . iv) the claimed the memory port independent from the video input port, ... (Office Action pp. 11-12).
In regard to (iv), Agarwal teaches that the encoded image may then be stored to memory device 112 via bus 108, bus interface 110, and system bus 114 for storage in host memory 126, pixel processor 106 also may contain local memory 130, which is a tightly-coupled on-chip memory suitable for locally storing a number of pixels and their data, those skilled in the art will appreciate that system bus 114 and bus 108 may be merged into the same system bus 114 (FIG. 1, col. 4, lines 20-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the two system bus 114 and 108 as taught by Agarwal into Dea's system since it merely amount of selecting available buses. (Office Action pp. 13-14).

Therefore, any such teaching must be found in the newly cited reference, Agarwal. That is to say, Agarwal would have to teach the missing elements of Applicant's amended independent claim 13, namely

a memory port coupled to the previous frame buffer and the result buffer, the memory port independent from the video input port; and

a system memory ***coupled to the memory port for storing the video data from the video input port and the difference frame from the result buffer***, wherein the video data is stored to in a current frame in the memory, the apparatus configured to operate within a north bridge chip of the computer system ***to enable the central processing unit via the north bridge chip to retrieve the difference frame exclusive of a system bus directly from the system memory via the north bridge chip*** for further compression of the video data by the central processing unit.

While the Office Action makes statements that Agarwal teaches the missing elements, the Office Action mischaracterizes the teachings of the Agarwal reference which, in fact, does not teach the missing elements.

While the Office Action states:

> 1) Agarwal teaches that the encoded image may then be stored to memory device 112 via bus 108, bus interface 110, and system bus 114 for storage in host memory 126, pixel processor 106 also may contain local memory 130, which is tightly-coupled on-chip memory suitable for locally storing a number of pixels and other data, those skilled in the art will appreciate that system bus 114 and bus 108 may be merged into the same system bus 114 (Fig. 1, col. 4, lines 20-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention ***to incorporate the two system bus 114 and 108 as taught by Agarwal*** into Dea's system since it merely amount of selecting available buses. (Office Action pp. 13-14; emphasis added).

In referencing Agarwal's Fig. 1, and according to the Office Action's characterization, the data flow is from pixel processor 106, to bus 108, to memory device 112, back to bus 108, to bus interface 110, to system bus 114, to host memory 126. Then, and only then, can host processor 116 retrieve data from host memory 126 for any further performance of video compression. It should be noted that such a retrieval of data necessitates traversal of the system bus at least on two separate occasions. The Applicant's invention as claimed, allows the "central processing unit to retrieve the difference frame exclusive of the second bus and directly from the system memory" wherein the second bus is configured in a manner similar to a "system bus".

While the Office Action and the Agarwal reference state that the "system bus 114 and bus 108 may be merged into the same system bus 114", such a configuration places pixel processor 106, memory device 112, system memory 126 and host processor 116 all on a single system bus 114 which is in contradiction to the lack of teaching of Applicant's claimed invention of:

> a memory port coupled to the previous frame buffer and the result buffer, the memory port independent from the video input port; and
>
> a system memory ***coupled to the memory port for storing the video data from the video input port and the difference frame from the result buffer***, wherein the video data is stored to in a current frame in the memory, the apparatus configured to operate within a north bridge chip of the computer system ***to enable the central processing unit via the north bridge chip to retrieve the difference frame***

exclusive of a system bus directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit.

Therefore, Applicant respectfully requests that the rejection to amended independent claim 13 be withdrawn. Furthermore, claim 14 through 16 and 18 through 19 depending from amended independent claim 13 are also allowable as depending from allowable amended independent claim 13.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 5,909,559 to So, U.S. Patent No. 6,246,719 to Agarwal and further in view of U.S. Patent No. 5,438,374 to Yan

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559), Agarwal (U.S. Patent No. 6,246,719) and further in view of Yan (U.S. Patent No. 5,438,374). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant respectfully requests that the rejection to claim 9 be withdrawn for at least the reason that it depends from now-allowable independent claim 1.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 5,909,559 to So, U.S. Patent No. 6,246,719 to Agarwal and further in view of U.S. Patent No. 5,926,223 to Hardiman

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559), Agarwal (U.S. Patent No. 6,246,719) and further in view of Hardiman (U.S. Patent No. 5,026,223). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant respectfully requests that the rejection to claim 11 be withdrawn for at least the reason that it depends from now-allowable independent claim 1.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 5,909,559 to So, U.S. Patent No. 6,246,719 to Agarwal, U.S. Patent No. 4,546,383 to Abramatic et al. as applied to claim 13 above, and further in view of U.S. Patent No. 5,438,374 to Yan

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559), Agarwal (U.S. Patent No. 6,246,719), Abramatic et al. (U.S. Patent No. 4,546,383) as applied to claim 13 above, and further in view of Yan (U.S. Patent No. 5,438,374). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant respectfully requests that the rejection to claim 18 be withdrawn for at least the reason that it depends from now-allowable independent claim 13.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 5,909,559 to So, U.S. Patent No. 6,246,719 to Agarwal, U.S. Patent No. 4,546,383 to Abramatic et al. as applied to claim 13 above, and further in view of U.S. Patent No. 5,926,223 to Hardiman

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559), Agarwal (U.S. Patent No. 6,246,719), Abramatic et al. (U.S. Patent No. 4,546,383) as applied to claim 13 above, and further in view of Hardiman (U.S. Patent No. 5,926,223). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant respectfully requests that the rejection to claim 19 be withdrawn for at least the reason that it depends from now-allowable independent claim 13.

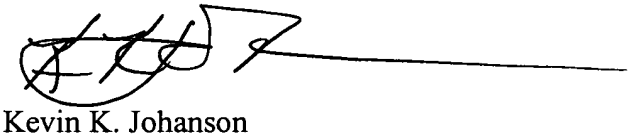
ENTRY OF AMENDMENTS

The amendments to claims 1 and 13 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search.

CONCLUSION

Claims 1 through 7, 9through 16, 18 and 19 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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